REMARKS

Claims 1-31 are pending. Claims 1-31 are rejected. In the previous Office Action, claims 1-11 were rejected under 35 USC 103(a) as being unpatentable over Self (5,623,644) in view of Booth (6,065,073) and further in view of Ren (Using Clustering for Effective Management of a Semantic Cache in Mobile Computing). In the previous Office Action, claims 12-31 were rejected under 35 USC 103(a) as being unpatentable over Self in view of Kelly (5,379,440), Booth, Dervin (6,952,766), and Sgroi "Addressing the System-on-a-chip Interconnection Woes Through Communication-Based Design." In light of the previous response to Office Action, the Examiner is now providing new grounds of rejection.

The Examiner objected to the drawings as not showing particular reference signs. Replacement sheets for Figures 7-9 are being provided that correspond with the description associated with Figures 7-9. It is respectfully submitted that no new matter is being introduced. For example, replacement sheet Figure 7 merely shows the components described in the description of Figure 7. "In one example, configuration space registers 701 include a physical layer indicator 711 to enable or disable physical layer communications... According to various embodiments, configuration space registers 701 also include a link layer indicator 713. In one example, the link layer indicator 713 is a fence bit... According to various embodiments, the configuration space registers also include a reinitialize indicator 715 to indicate whether or a new initialization sequence should be performed. Registers for holding cluster identifiers 717, 719, and 721 also are provided to allow configuration space registers 701 to maintain the IDs of connected clusters. It should be noted that not all of the values in the configuration space registers 701 are necessary." (page 16, line 23 – page 17, line 23)

Replacement sheets for figures 8 and 9 show flow process diagrams corresponding to the descriptions of Figures 8 and 9. "At 801, physical layer communications are enabled out of reset. Standard physical layer initialization sequences can be performed upon enabling the physical layer... At 803, a fence bit is set to disable link layer communications... At 805, the initialization sequence or a training sequence is transmitted... At 811, link width parameters are exchanged. At 813, link speed parameters are exchanged. At 815, optional error correction information is exchanged. At 817, the link layer is then enabled by toggling the fence bit off. With the link layer enabled, data communications can proceed. At 819, cluster ID information is

exchanged. At 821, the cluster ID is set in the configuration space registers. At 823, routing tables associated with the interconnection controllers are updated as needed to reflect connected resources." (page 17, line 29 – page 18, line 29) Similarly for Figure 9, "Figure 9 is a flow process diagram showing use of space registers during hot plugging... At 901, the polling state is maintained at an interconnection controller. At 903, a fence bit is maintained to disable the link layer. It should be noted, however, that a fence bit does not necessarily have to be disabled. When a new processing cluster is detected, a reinitialization is triggered at 905... At 907, initialization sequences or training sequences are sent. At 911, information such as link width and links speed is exchanged. The link layer is then enabled at 913. At 915, the cluster ID of the newly added group of processors is written to the configuration space registers. At 917, routing tables described above are similarly updated to allow multiple cluster communications." (page 20, lines 2-13)

To facilitate prosecution, claims 1-31 have been canceled. Claims 32-51 are new. Various objections raised by the Examiner are believed moot in light of the newly provided claims. Claims 32-51 are supported by the original claims and the specification. For example, Claims 32-51 are supported by Figure 10 and associated description. "Figure 10 is a flow process diagram showing a technique for dynamically removing resources from a system. It is typically difficult to dynamically unplug resources such as processors or processing clusters while a system is active because removing processors and their associated caches critically affects system operation. In one example, data being processed by a particular application may be held in an intermediate state in processor caches to be removed from a system. Similarly, an operating system processes may be running on one or more processors set for removal. According to various embodiments, an operating system supporting dynamic removal of clusters would be used. In one example, applications are terminated at 1001 in an operating system environment that supports dynamic removal of multiprocessor clusters. A cluster is disabled at 1003 but not yet unplugged. At 1005, caches associated with the cluster to be removed are flushed. At 1007, routing tables are modified to reflect the removal of a processing cluster. At 1009, a fence bit is written in the configuration space registers. A fence bit may be written by a variety of entities. In one example, the fence bit is written by a service processor or by a JTAG interface associated with a processor. At 1011, the multiple processor cluster can be physical removed. At 1013, the physical layer at the interconnection controller still residing in the system

may be maintained in order to allow for a new or replacement cluster of processors to be introduced." (Figure 10 Description)

Furthermore, "a fence bit is set to disable link layer communications. Disabling link layer communications allows physical layer communications to be established without interference from data local transmissions. It should be noted, however, that link layer communications do not necessarily have to be disabled." (page 18, lines 3-7)

None of the references cited by the Examiner either alone or in combination teach or suggest the recited elements of the new independent claims. For example, none of the reference cited either alone of in combination are believed to teach or suggest "disabling link layer communications associated with the first processor cluster, wherein the first processor cluster is disconnected after disabling link layer communications associated with the first processor cluster" and "maintaining physical layer communications associated with the first processor cluster to allow connection of a replacement processor cluster."

In light of the above remarks, the rejections to the independent claims are believed overcome for at least the reasons noted above. Applicants' Representative believes that all pending claims are allowable in their present form. If the Examiner has any questions or concerns for Applicants' Representative, the Examiner is encouraged to contact the Undersigned at the number provided below. If any fees are due in connection with this filing, the Commission is authorized to charge Deposit Account No. 504480. (Reference No. NWISP046)

Respectfully submitted,
Weaver Austin Villeneuve & Sampson LLP

/Audrey Kwan/

G. Audrey Kwan
Reg. No. 46,850

P.O. Box 70250
Oakland, CA 94612-0250
(510) 663-1100